

JK, RS, T Flip-Flop Design

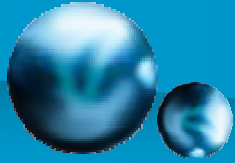
Design Practice - MyCAD



Table of Contents



- **Preface**
- **NAND2 Design**
 - **NAND2 schematic and symbol**
 - **NAND2 simulation**
 - **NAND2 layout and results of verification**
- **NAND3 Design**
 - **NAND3 schematic and symbol**
 - **NAND3 simulation**
 - **NAND3 layout and results of verification**
- **JK Flip-Flop Design**
 - **JK Flip-Flop schematic and symbol**
 - **JK Flip-Flop simulation**
 - **JK Flip-Flop layout and results of verification**
- **RS Flip-Flop Design**
 - **RS Flip-Flop schematic and symbol**
 - **RS Flip-Flop simulation**
 - **RS Flip-Flop layout and results of verification**
- **T Flip-Flop Design**
 - **T Flip-Flop schematic and symbol**
 - **T Flip-Flop simulation**
 - **T Flip-Flop layout and results of verification**

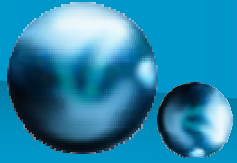


Preface



- This document provides the information on how to design JK, RS, T Flip-Flop schematic and layout.
- JK, RS, T Flip-Flop is designed based on MOSIS SCMOS layout rules.
- If you want to get more information, please refer to the related documents as below.
 - **MyCAD Tutorial :**
Learn how to use schematic and layout editor.
 - **MySpice Tutorial :**
Learn about simulating a circuit.
 - **MyChip Pro Verification Reference Manual :**
Look up specific verification commands.

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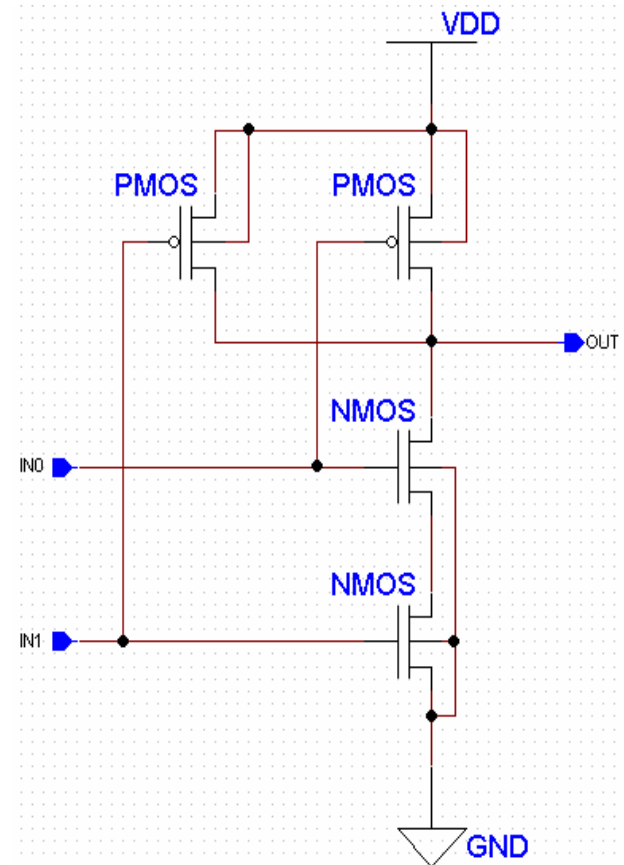
NAND2 schematic and symbol



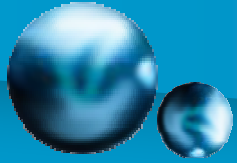
Logic Symbol

IN0	IN1	OUT
0	0	1
0	1	1
1	0	1
1	1	0

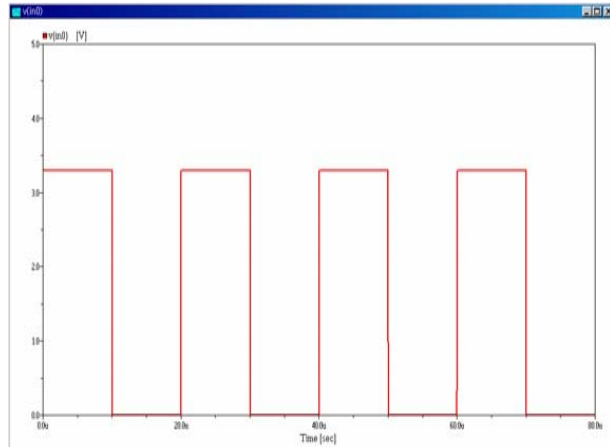
Truth Table



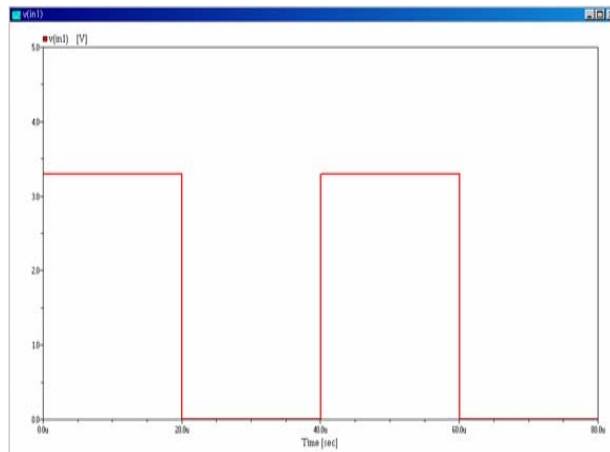
Schematic



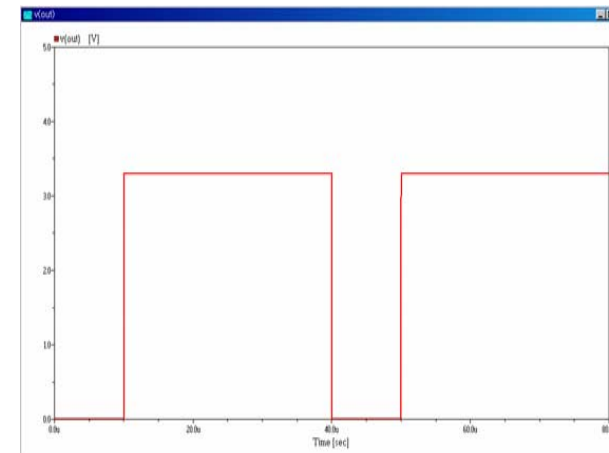
NAND2 Simulation



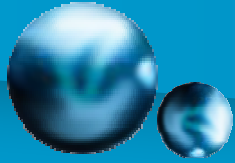
INO



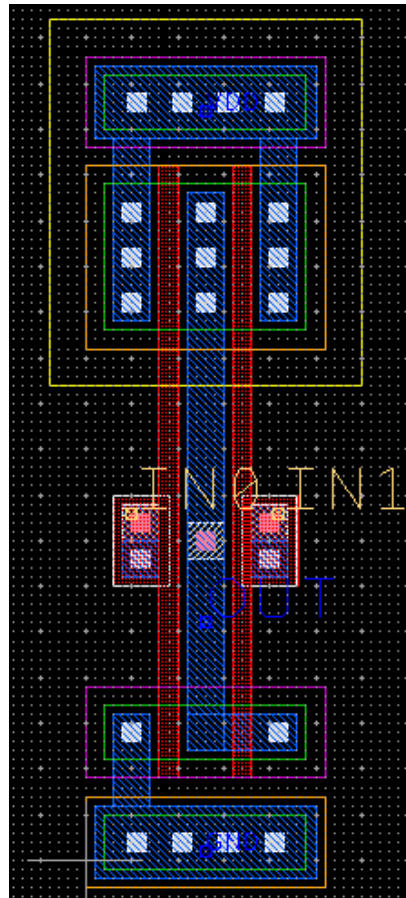
IN1



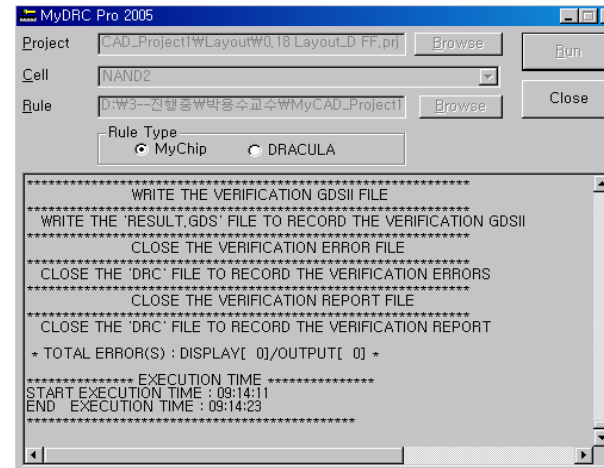
OUT



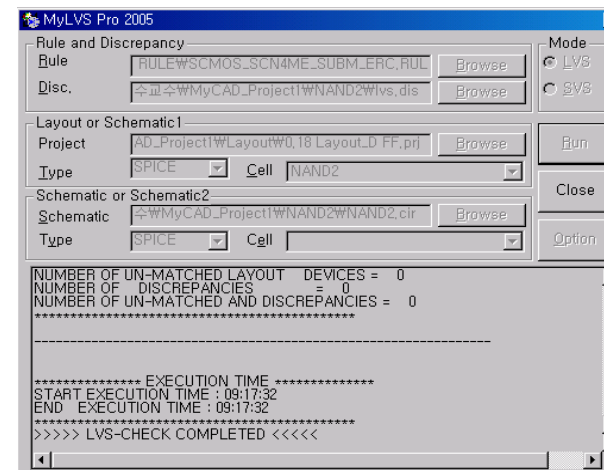
NAND2 layout and results of verification



Layout



DRC result



LVS result



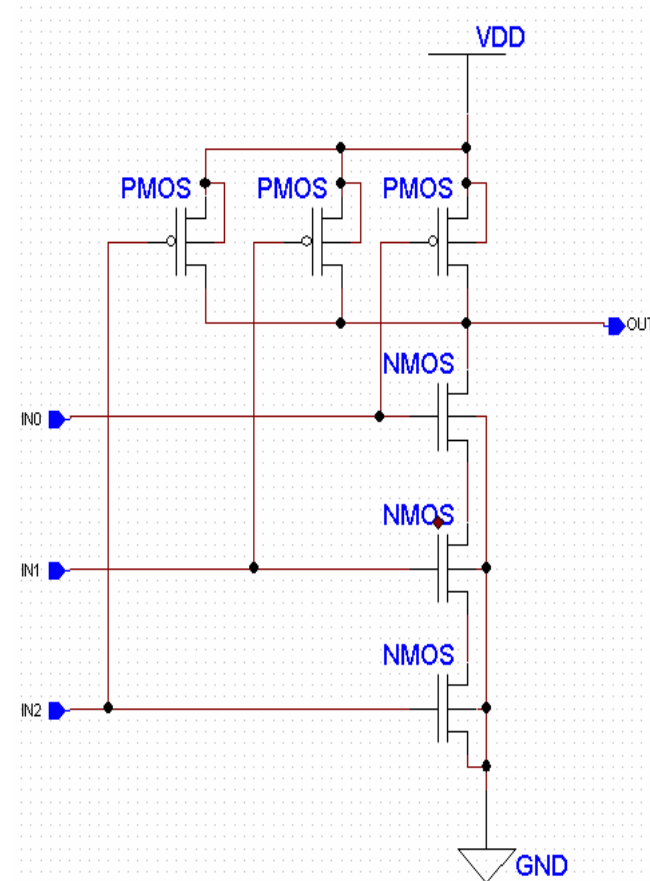
NAND3 schematic and symbol



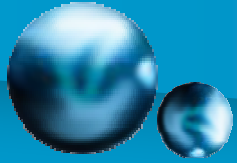
Logic Symbol

Input			Output
A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

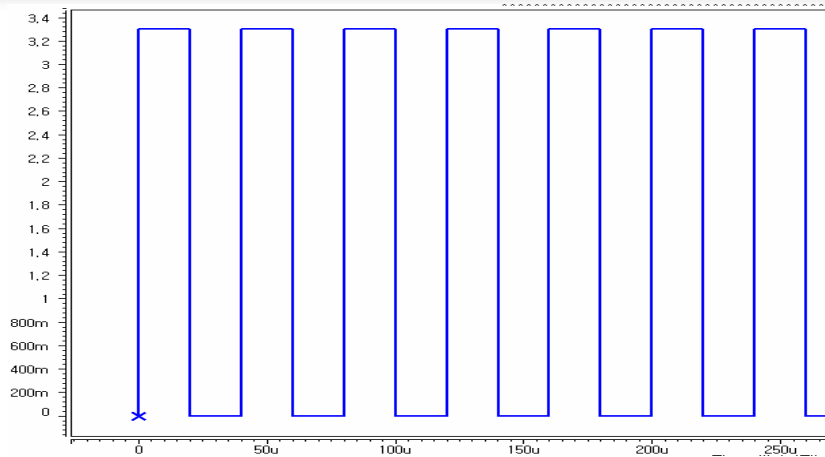
Truth Table



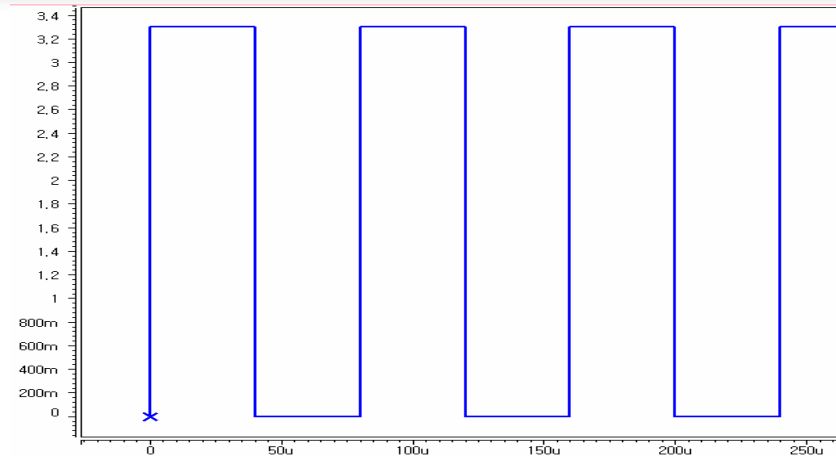
Schematic



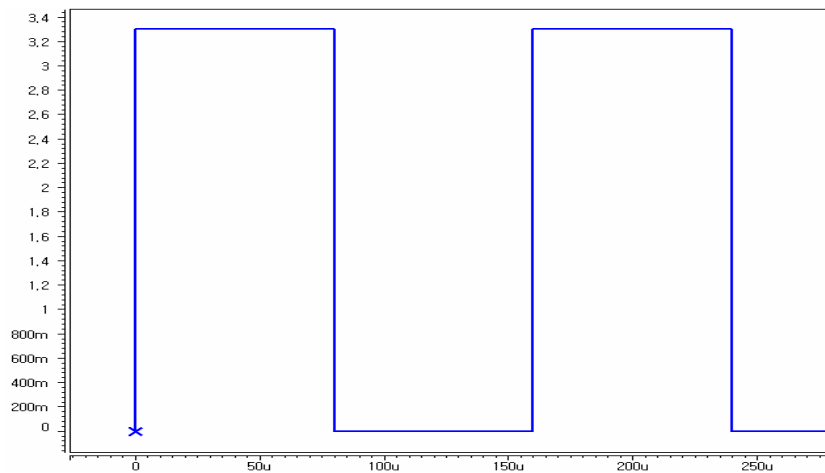
NAND3 Simulation



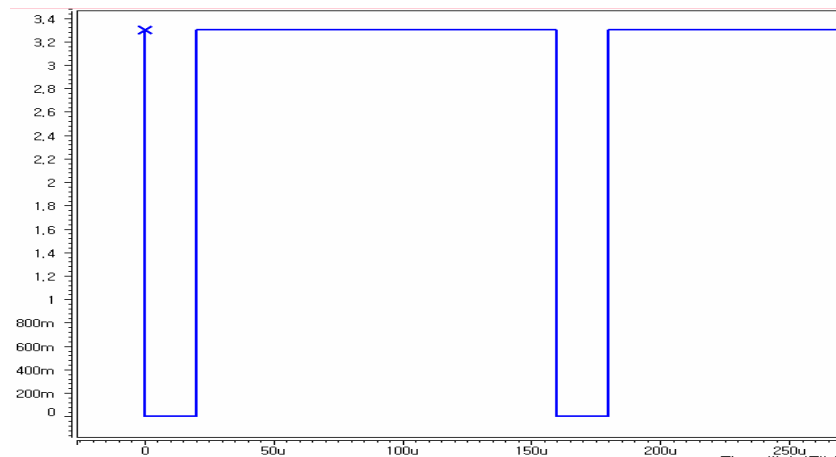
IN0



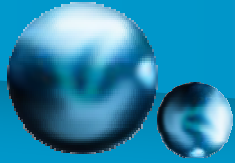
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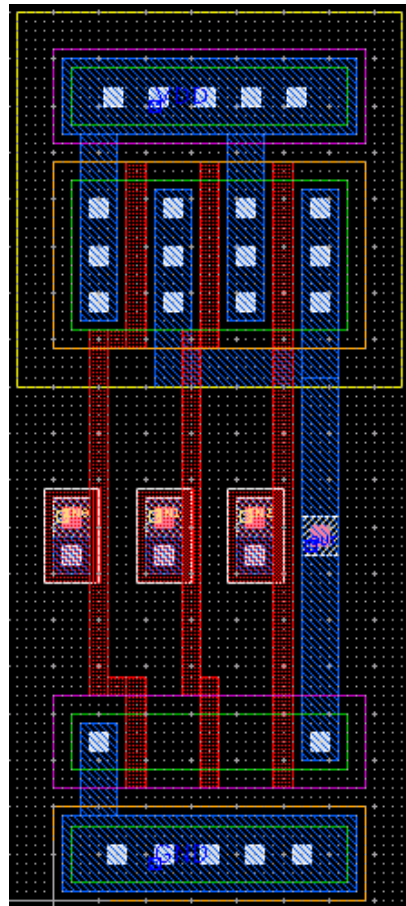
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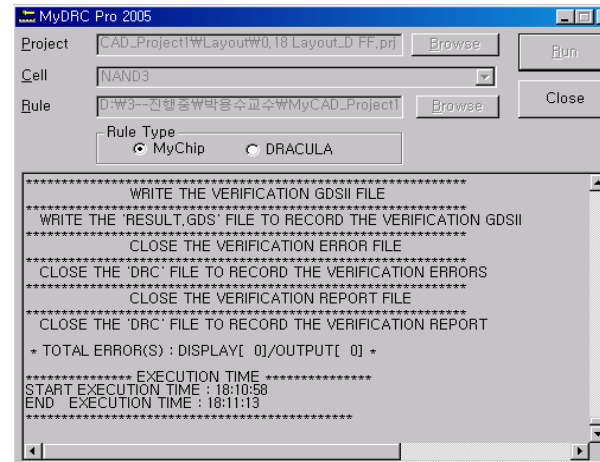
OUT



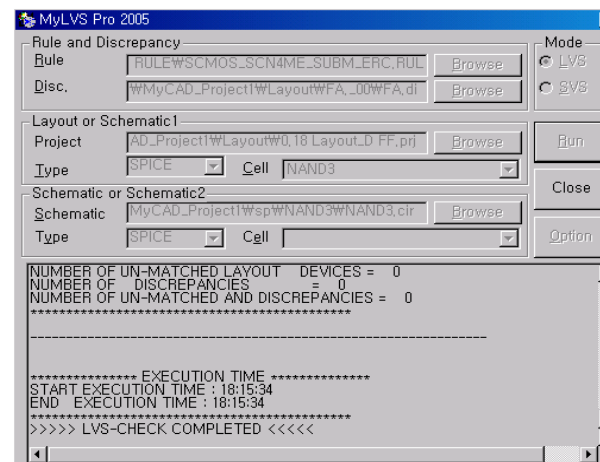
NAND3 layout and results of verification



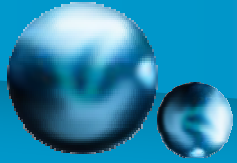
Layout



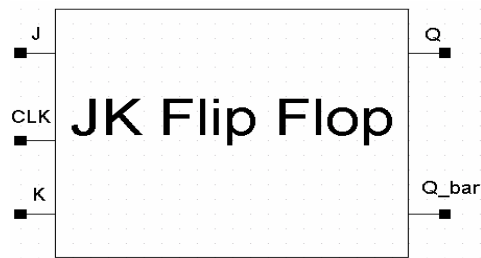
DRC result



LVS result



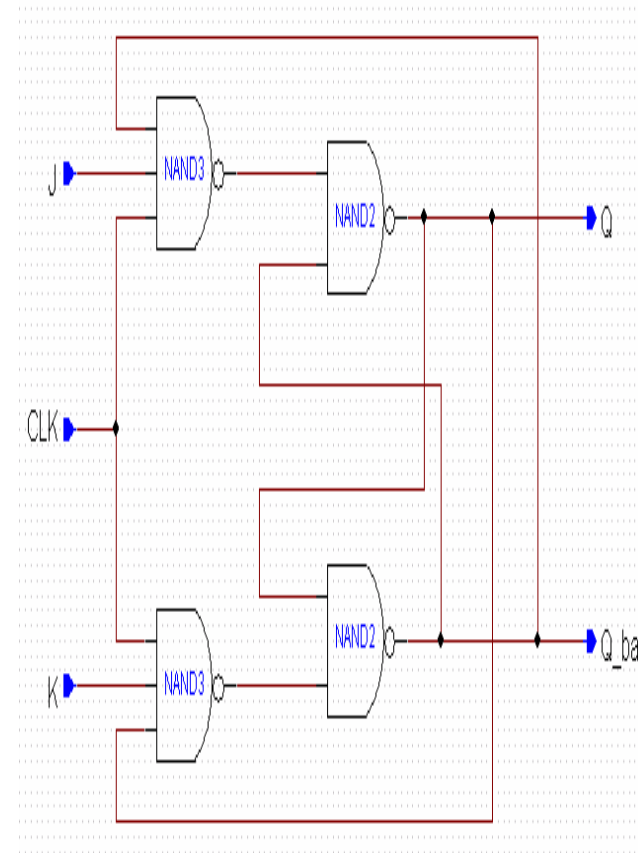
JK FF schematic and symbol



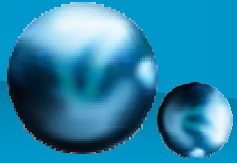
Logic Symbol

Input		Output	
J	K	Q _{n+1}	동작
0	0	Q _n	불변
0	1	0	리셋
1	0	1	세트
1	1	Q _n '	반전

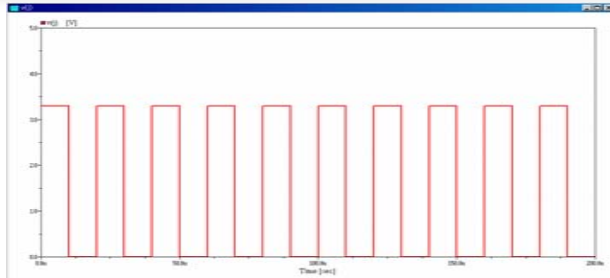
Truth Table



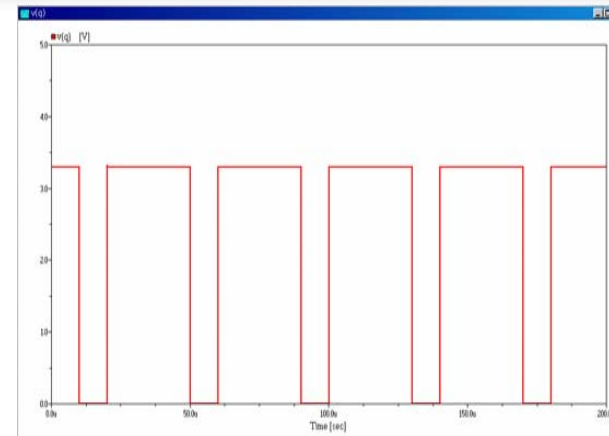
Schematic



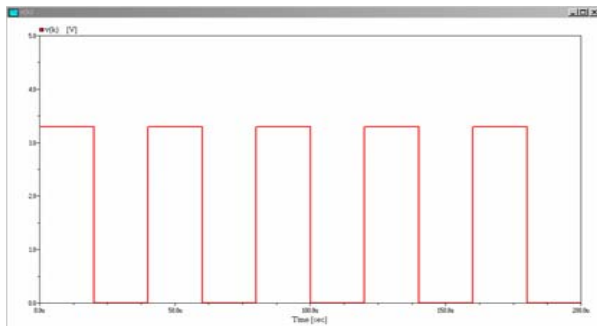
JK FF Simulation



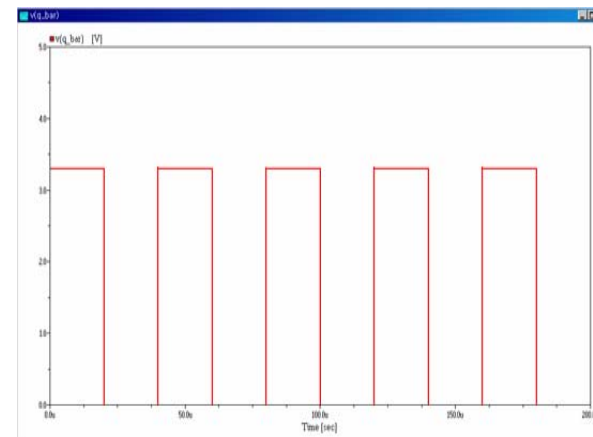
J



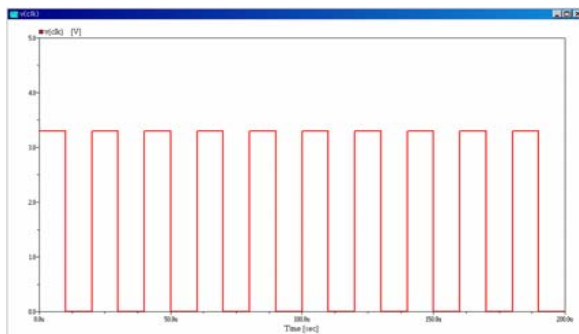
Q



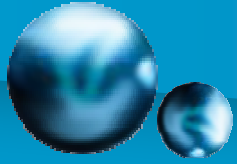
K



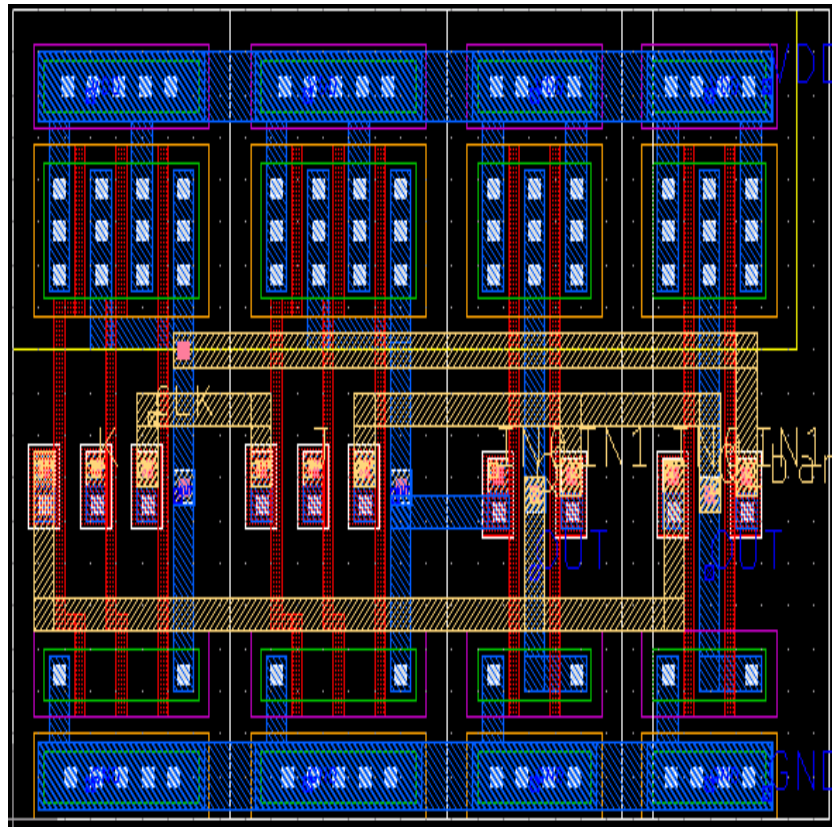
Q_bar



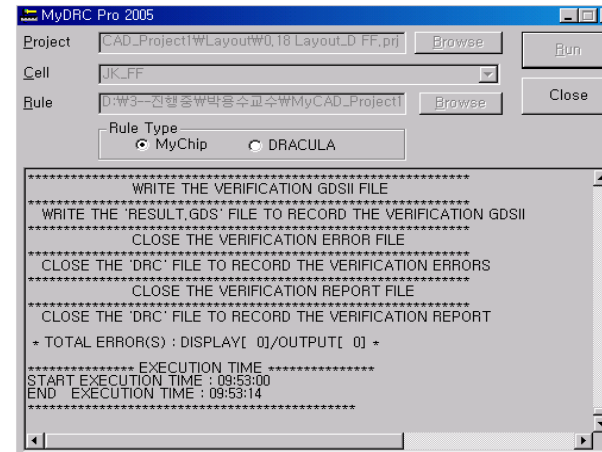
CLK



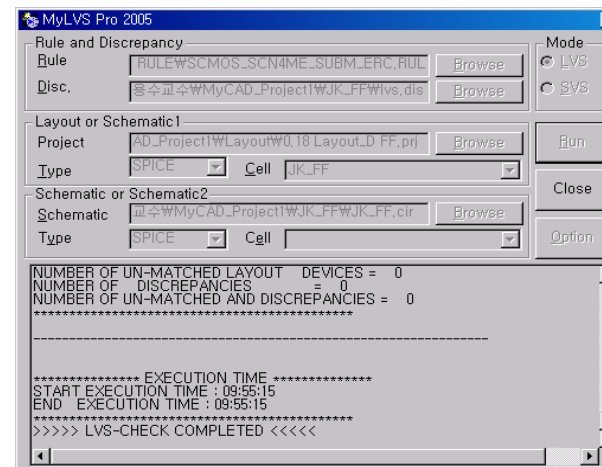
JK FF layout and results of verification



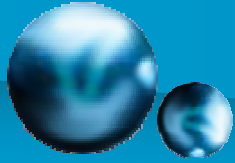
Layout



DRC result



LVS result



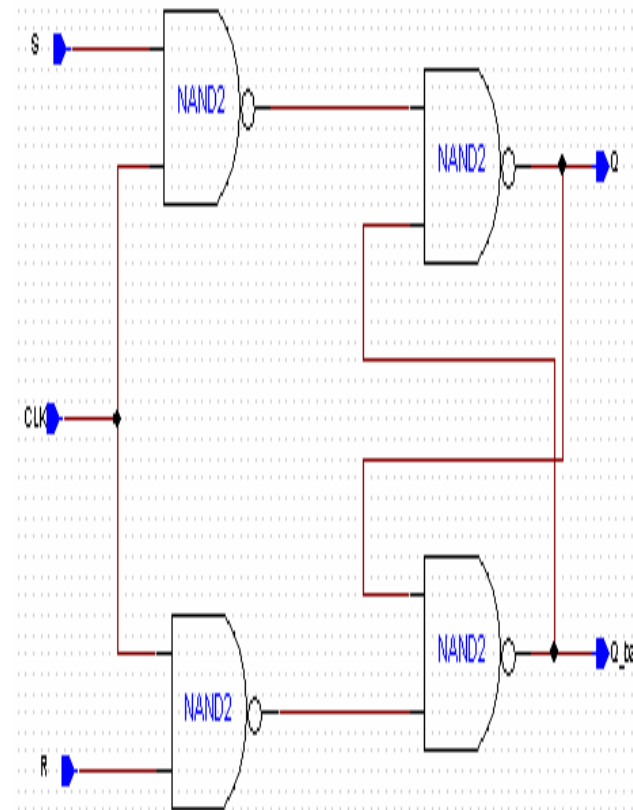
RS FF schematic and symbol



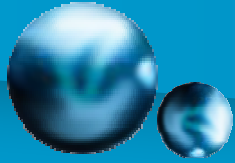
Logic Symbol

Input		Output	
S	R	Q	동작
0	0	전 상태유지	
0	1	0	리셋
1	0	1	세트
1	1	사용불가	

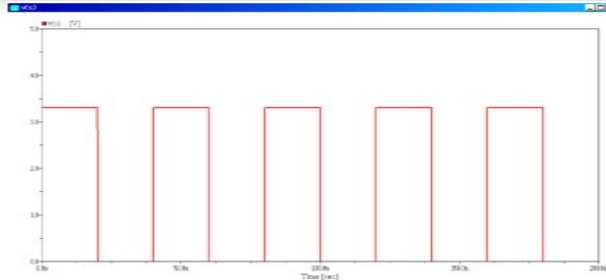
Truth Table



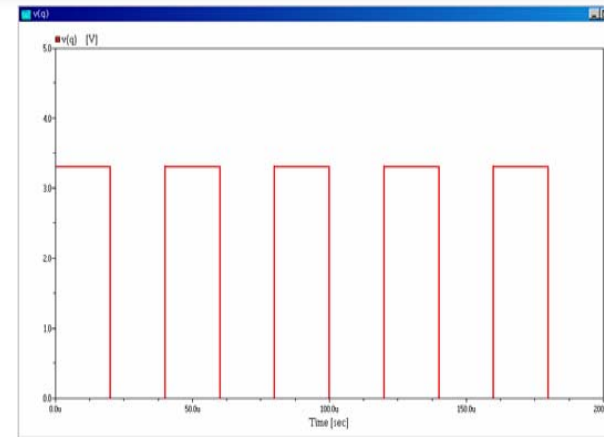
Schematic



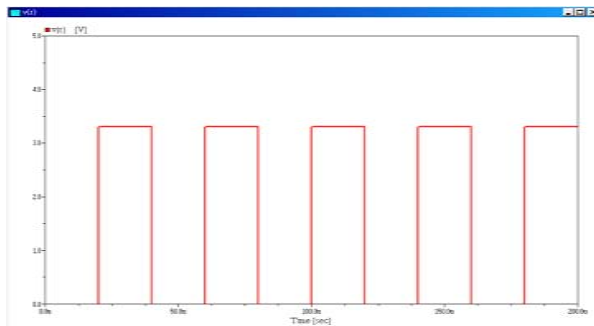
RS FF Simulation



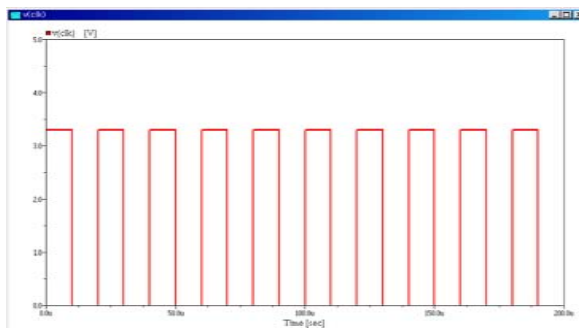
S



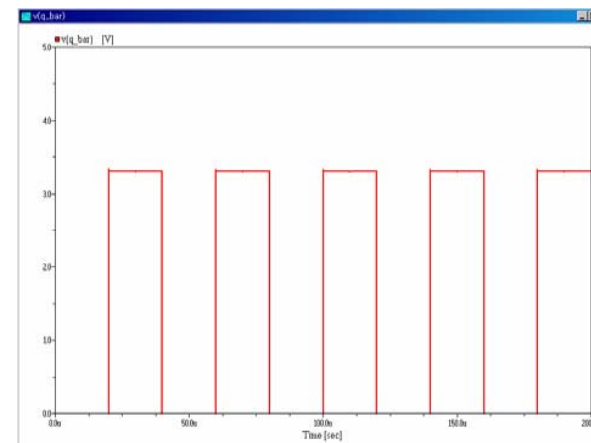
Q



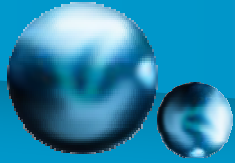
R



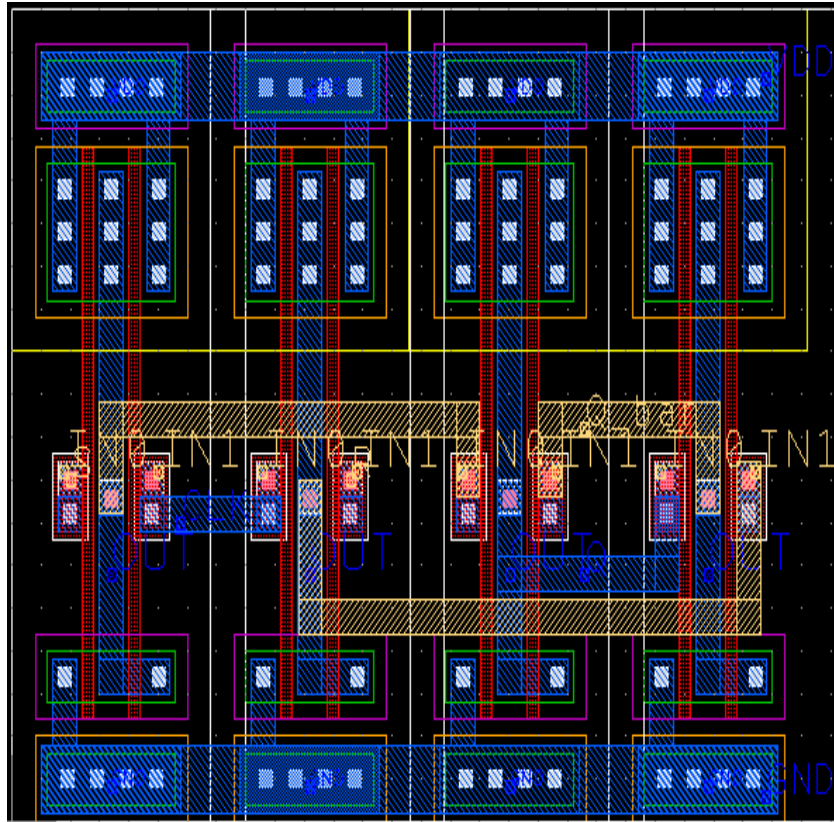
CLK



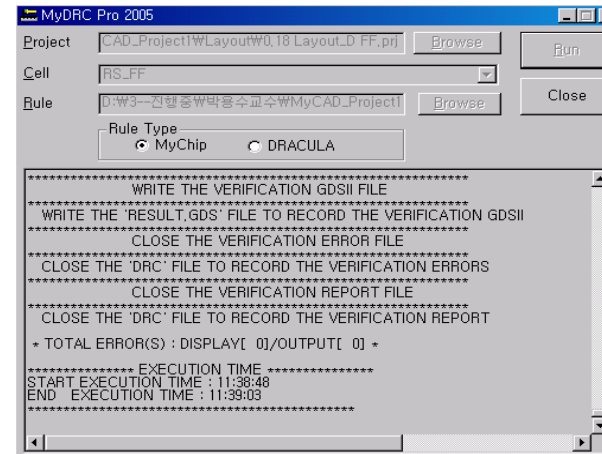
Q_bar



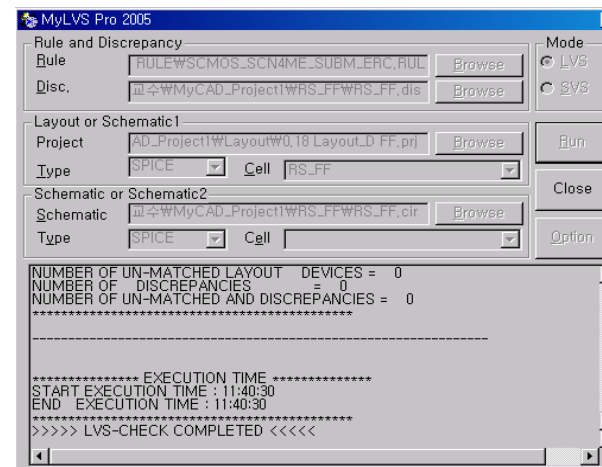
RS FF layout and results of verification



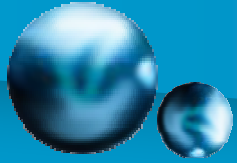
Layout



DRC result



LVS result



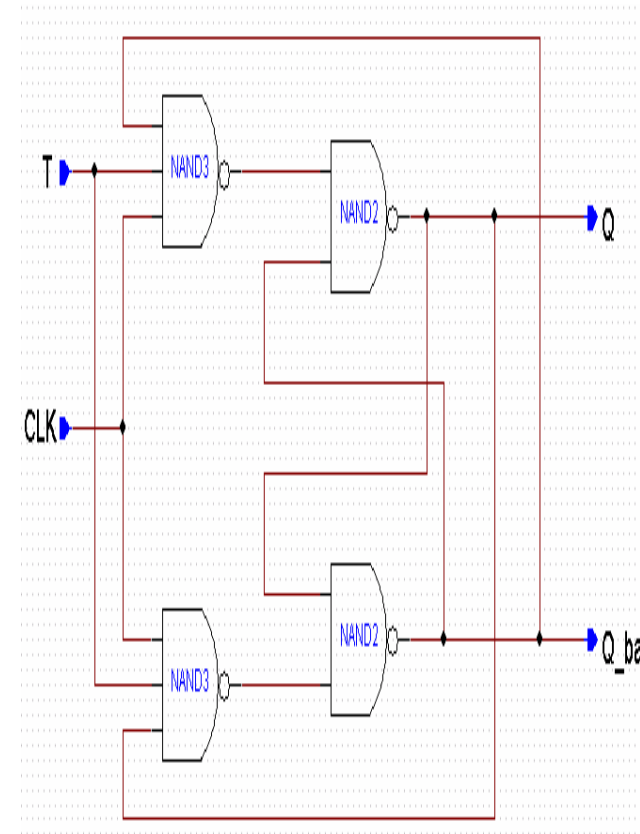
T FF schematic and symbol



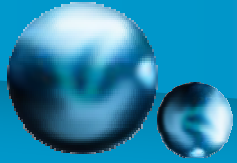
Logic Symbol

Input	Output
T	Q
0	Q ⁰
1	Q ^{0'}

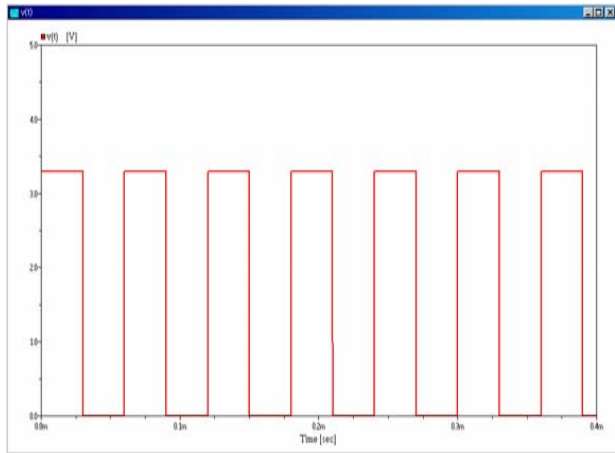
Truth Table



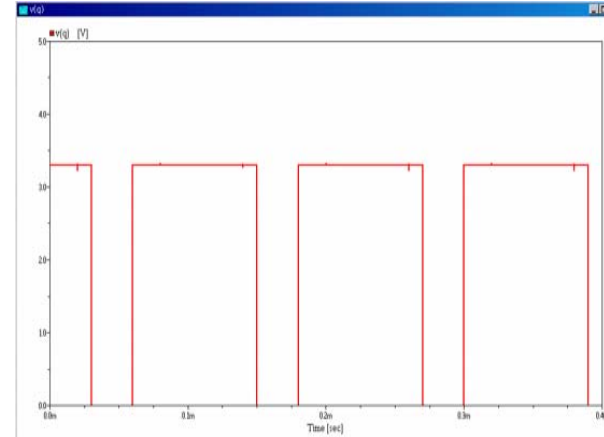
Schematic



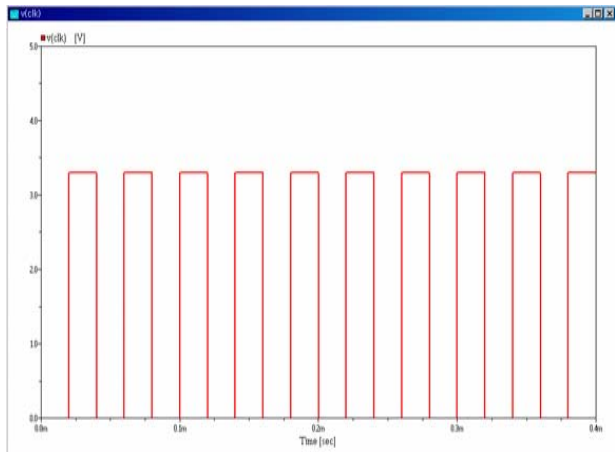
T FF Simulation



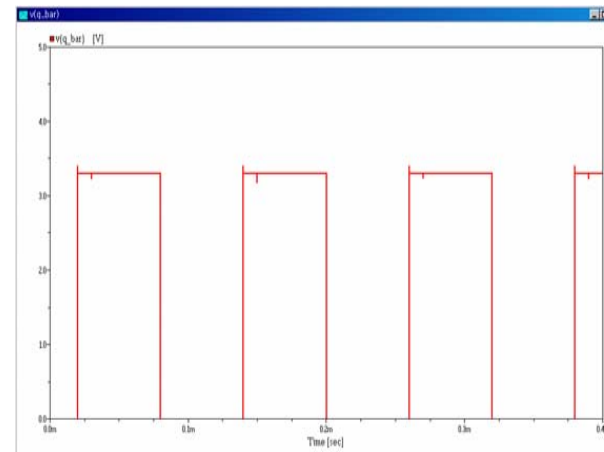
T



Q



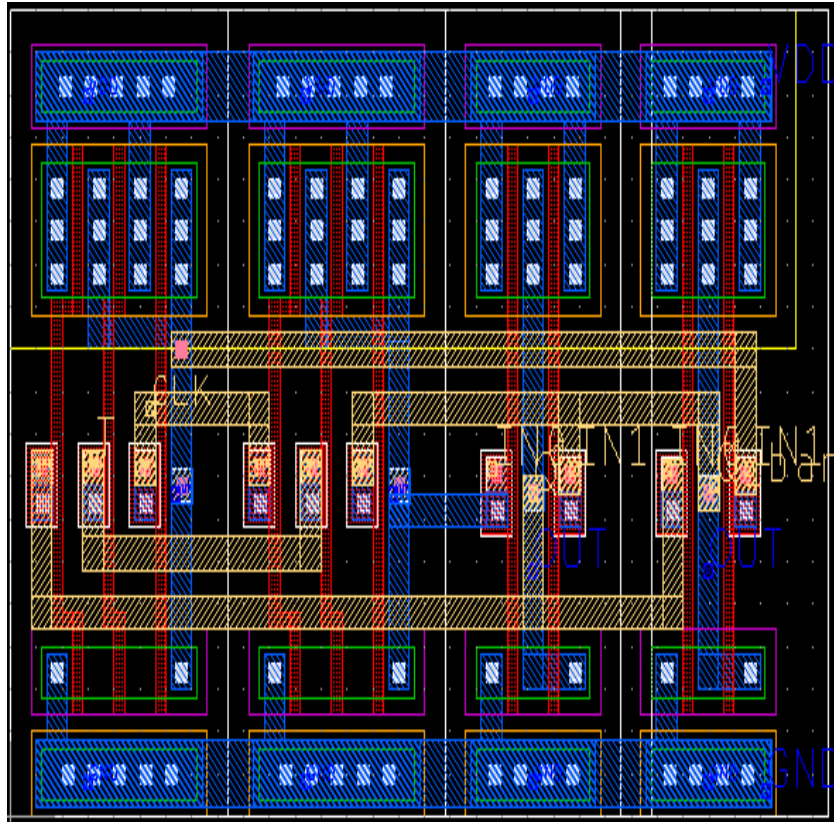
CLK



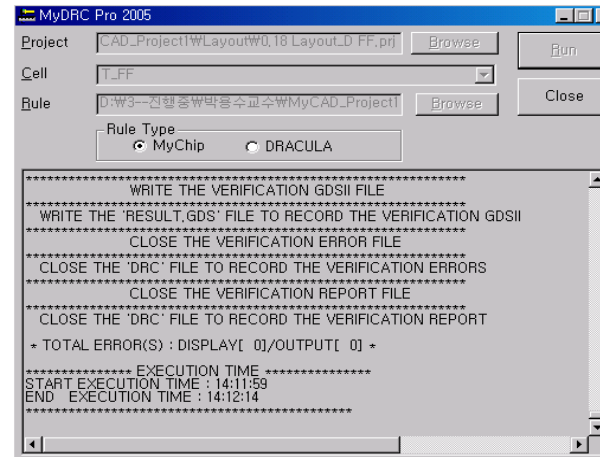
Q_bar



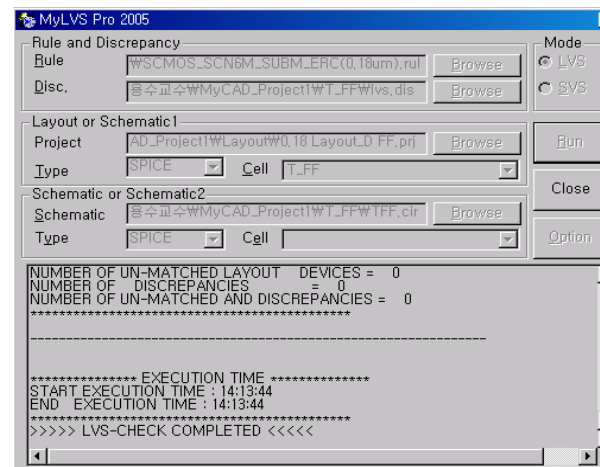
T FF layout and results of verification



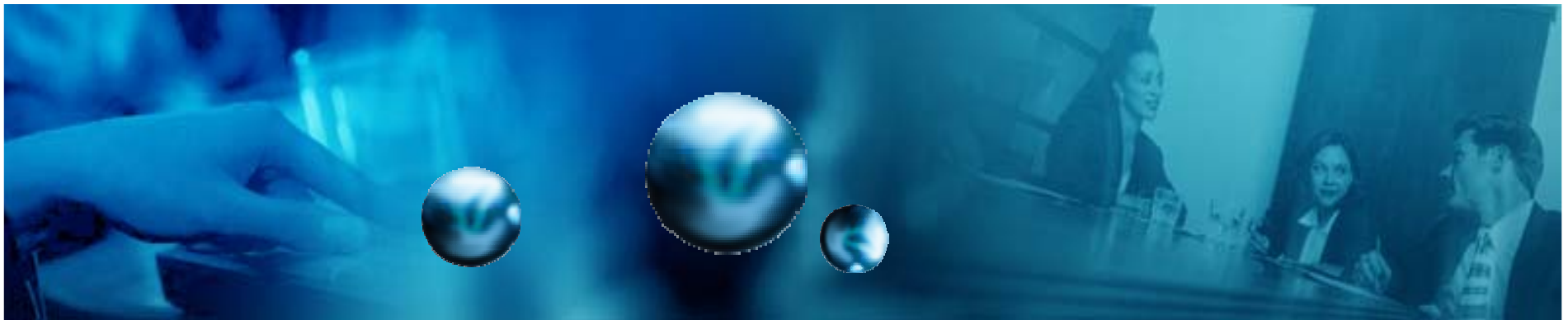
Layout



DRC result



LVS result



The End